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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
09/028,456	02/24/98	OHASHI	Y	JAO-40656

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/028,456	Applicant(s) Ohashi
	Examiner Luan Thai	Group Art Unit 2811

☒ Responsive to ~~communication(s) filed on~~ *the amendment filed on August 31, 1999* .

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-23* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-23* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *7*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

This Office action is responsive to the amendment filed August 31, 1999.

Claims **1-23** are pending in this application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **1-7** and **15-23** are rejected under 35 U.S.C. 102(b) as being anticipated by Higgins (5,212,402) (as set forth in the previous Office Action paper Number 6 and now repeated).

With respect to claims **1, 4-5, 15-16, 18**, and **20-21**, Higgins discloses (see figures 1-3, 5, and 15-16) specifically see figure 1, a tape carrier package semiconductor device comprising a semiconductor chip (38) having pads 52 (see figure 5) formed thereon; a flexible insulation substrate (13) with conductor patterns for power source (19), grounding (36), and signal (16) formed thereon; and a sealing resin 58 (see figure 8), wherein the conductor patterns protrude into an opening (20) defined in the flexible insulation substrate and are coupled to the semiconductor chip in a coupling section (see figures 8-10), the coupling section being sealed by the sealing resin (see figures 8-10), and wherein the conductor pattern (19 or 36) extends across the opening and has a width wider than a width of one of the pads of the semiconductor chip (see figures 2-3 and 15-16), the conductor pattern (19 or 36) extends across the opening has a connection branch (see figures 2-3) which has a tip section connected to the flexible insulation substrate, the connection branch having a width narrower than a width of one of the pads of the semiconductor chip (see figures 15-16).

With respect to claims **2, 6, 17**, and **22**, Higgins further discloses the conductor pattern extending across the opening has one bent section (see figures 3, 5, 11-13, 15-16).

With respect to claims **3, 7, 19**, and **23**, although Higgins does not specifically disclose that the semiconductor device as detailed above is a part of an electronic device, the semiconductor device would inherently be part of a larger device or an electronic device since at least a means for providing a voltage is disclosed and it is apparent that some type of power source and some type of other electronic component (such as signal source) must be present for the device to function as intended.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **8-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Higgins (5,212,402) (as set forth in the previous Office Action paper Number 6 and now repeated).

Higgins discloses (see figures 1-3, 5, and 15-16) specifically see figure 1, all the features of the claimed invention as detailed above except for teaching that at least one of the power source electrode and the grounding electrode of the semiconductor chip is larger than the signal electrode. However, making the power source electrode or the grounding electrode of the semiconductor chip to be larger than the signal electrode could increase the current carrying capacity of the electrode and this would have been obvious to a person of ordinary skill in the art. Moreover, it would have been an obvious matter of design choice to form the power source electrode or the grounding electrode of the semiconductor chip to be larger than the signal electrode since such a modification would have involved a mere change in the size of a

component. A change in size is generally recognized as being within the level of ordinary skill in the art. In addition, forming the power source electrode or the grounding electrode of the semiconductor chip to be larger than the signal electrode is conventional in semiconductor art in order to improve the current carrying capacity of the electrode. Note Atsushi (JP 08316270, figure 2) and Inoue (JP 01289276, figures 1 and 3) are cited to support the well known position.

Response to Arguments

3. Applicant's arguments filed on August 31, 1999 have been fully considered but they are not persuasive. Specifically:

(a) Applicant argues, at page 2 of the Remarks, that Higgins does not disclose or suggest conductor patterns extending across an opening having a width wider than the width of one of the pads of the semiconductor chip, as recited in claim 1.

In response, the Examiner points out that Higgins does show the conductor patterns 19 (figure 2), 36 (figure 3), 68 (figure 15) or 68, 78 (figure 16) extend across an opening, and at least a portion of these conductor patterns has a width wider than the width of the pad of the semiconductor chip (note in figure 5, portion 37 is wider than pads 52; in figure 15, portion 69 is wider than pads 74; in figure 16, portions 69 and 79 are wider than pads 74).

(b) Applicant argues, at page 3 of the Remarks, that Higgins does not disclose or suggest 1) at least one of the conductor patterns having at least one connection branch, the connection branch having a width narrower than a width of one of the pads of the semiconductor chip, as recited in claims 4, 2) at least one of the conductor patterns having at least one branch, the branch having a tip portion connected to a flexible insulation substrate as recited in claim 15, or 3) each of the conductor patterns having at least one branch connection inner lead, the branched connection inner lead having a width narrower than the width of one of the pads of the semiconductor chip, as recited in claim 20.

In response, the Examiner points out that Higgins does show 1) the conductor patterns 23 (figure 2) and 37 (figure 3) having connection branches 19 and 36 respectively wherein these branches have a width narrower than a width of one of the pads (see figures 15-16) of the semiconductor chip (note that branches 78 and 68 of conductor patterns 79 and 69 respectively (in figure 16) are perspective views illustrating in according with the plan view of the branches 19 and 36 of conductor patterns 23 and 37 respectively (in figures 2 and 3); 2) the conductor pattern 23 (see figure 2) has branches 19 which have a tip portion connected to a flexible insulation substrate 13; and 3) each of conductor patterns 23 (figure 2) and 37 (figure 3) have connection branch connection inner leads 19 and 36 respectively, wherein these branch connection inner leads have a width narrower than the width of one of the pads of the semiconductor chip (see figures 15-16).

(C) Applicant argues, at the last paragraph of page 3 of the Remarks, that Higgins does not disclose or suggest at least one of the power source electrode and the grounding electrode of the semiconductor chip being larger than the signal electrode, as recited in claim 8.

In response, the Examiner points out that although Higgins does not disclose the power source electrode or the grounding electrode of the semiconductor chip being larger than the signal electrode, forming the power source electrode or the grounding electrode to be larger than the signal electrode is conventional in semiconductor art in order to improve the current carrying capacity of the electrode. Note Atsushi (JP 08316270, figure 2, previously applied) and Inoue (JP 01289276, figures 1 and 3, previously applied) are cited to support the well known position.

Conclusion

4. Applicant's arguments filed on August 31, 1999 have been fully considered but they are not persuasive. Therefore, **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

6. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to ***Luan Thai*** whose telephone number is **(703) 308-1211**. The Examiner is in the Office generally between the hours of 7:30 AM to 4:00 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **(703) 308-0956**.

Tom Thomas

Tom Thomas
Supervisory Patent Examiner
Technology Center 2800

10/20/99

Luan Thai